MEET UDESHI

+1-607-216-5524 m.udeshi@nyu.edu
mudeshi.in udiboy1209

New York University
PhD Student, ECE, CGPA: 4.0/4.0
CRRL + CCS
Advisors: Prof Farshad Khorrami and Prof Ramesh Karri

Research Interests: hardware security, reverse engineering, decompilation

PUBLICATIONS

N. K. Boran, S. Rathore, **M. Udeshi** and V. Singh, "Fine-Grained Scheduling in Heterogeneous-ISA Architectures," in IEEE Computer Architecture Letters, vol. 20, no. 1, pp. 9-12, 1 Jan.-June 2021

M. Udeshi, H. Garg, V. Baddi, P. Dwarakanath and S. Ladwa, "Low Power Object Tracking on AI100 using Kernelized Correlation Filters," in Qualcomm QBuzz Conference 2021 (won **Best Paper Award**)

RESEARCH AND WORK EXPERIENCE

PhD Project - REMaQE
Aug'22 - Present

Control/Robotics Research Lab, Center for Cybersecurity

- Designed REMaQE: reverse engineering math equations from binary executables
- Leveraged the **Angr symbolic execution** framework for analysis of binaries
- Devised an **automatic parameter analysis** methodology to extract input, output and constant parameters of a function
- Implemented an **algebraic simplification** algorithm to simplify symbolic expressions to human-friendly equations
- Generated a **dataset of math equations** compiled into approx. 20,000 binaries

Senior Engineer, Qualcomm R&D
Jul'19 - Jul'22

ML Compiler Team for Cloud AI100 Accelerator

- Worked on key aspects of AI100 compiler like multi-core, multi-thread data tiling, memory management, graph scheduling and operator fusion
- Innovated various **graph optimization techniques** applicable to 2D and 3D computer vision models, recommendation systems and autonomous driving tasks
- Contributed to the open-source **Pytorch Glow** compiler framework
- Deployed power efficient object tracking pipeline using **Kernelized Correlation Filters (KCF)** algorithm on AI100

Master's Thesis - Hardware Security
Aug'18 - Jun'19

Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Designed a **prefetcher disabling attack** to amplify cache side-channel leakage
- Achieved **99%** reduction in prefetches generated by **AES program**
- Implemented confidence measurement for **Gem5** stride and DCPT prefetcher
- Simulated a timing attack on the **re-order buffer** using **SNIPER** x86 simulator
- Implemented tools to reverse-engineer cache information of **Intel Skylake** cores

R&D Project - Heterogeneous-ISA Dynamic Core
Aug'17 - Jul'18

Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Implemented execution migration which helps HIDC switch between two ISAs
- Created a stack analysis and mapping framework for x86 and ARM using **LLVM**
- Proposed a granular function level migration strategy which reduces cost by **10x**
- Benchmarked the migration time between x86 and ARM using **Gem5** simulator

ACHIEVEMENTS

Awarded the **DAC Young Fellowship** to present a poster at DAC'23

Awarded the **Recognition of Outstanding Contributions (ROCStar)** for work on the AI100 compiler and KCF

Received a **Gold Medal** in Indian National Physics Olympiad

MENTORSHIP

Mentor for a hardware security project in the Qualcomm Innovation Fellowship from Aug'20 to May'21

Teaching Assistant for Microprocessor course (EE309) and VLSI Design lab (EE705) from Aug'18 to Apr'19

Manager of Electronics Club, IIT Bombay from May'16 to May'17

Reviewer in the 46th International Physics Olympiad

SKILLS

Relevant Courses

Hardware Security & Trust
Advanced Computer Architecture
Advanced Hardware Design
Deep Learning

Programming

Embedded C/C++	★★★★★
Python	★★★★★
Verilog/VHDL	★★★★☆

Frameworks

Angr Symbolic Exec	★★★★★
Pytorch Glow Compiler	★★★★☆
LLVM Compiler	★★★★☆
OpenCV	★★★☆☆

Tools

Ghidra	★★★★★
Vivado HLS	★★★★☆
Gem5	★★★★☆